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Gadolinium scandate thin films as an alternative gate dielectric prepared by electron beam evaporation

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Gadolinium scandate thin films deposited on silicon substrates using electron beam evaporation were investigated. Measurements with Rutherford backscattering spectrometry, high temperature x-ray diffraction, x-ray reflectometry, transmission electron microscopy, and atomic force microscopy were performed. A stoichiometric transfer of material from the source to the substrate in high vacuum could be demonstrated. Homogeneous, amorphous, and smooth films (root mean square surface roughness <1 Å) stable up to 1000 °C were obtained. Electrical characterization of capacitor stacks revealed a dielectric constant of ≈ 23, *C-V* curves with small hysteresises and low leakage current densities (770 $\mu A/cm^2$ for a capacitance equivalent thickness of 1.5 nm). © *2006 American Institute of Physics*. [DOI: 10.1063/1.2198103]

In order to satisfy the demand for higher performance and integration density in microelectronics, the scaling of metal oxide semiconductor field effect transistors (MOSFETs) becomes more and more aggressive. In this respect silicon dioxide as the gate dielectric will have to be replaced because of intolerable high leakage current densities. Therefore, one of the major challenges for the microelectronics industry is the integration of high-κ dielectrics into the complementary metal oxide semiconductor (CMOS) process in the near future.[1] A promising class of materials for high-κ applications are the rare earth scandates ($RE ScO_3$—*RE* denoting a rare earth element) because of their favorable material properties. For single crystals of these ternary oxides Schlom and Haeni[2] found dielectric constants of 20–35 depending on the lattice direction. Lim *et al.*[3] determined an optical band gap larger than 5 eV and Afanas'ev *et al.*[4] confirmed this value for thin amorphous films grown by pulsed laser deposition (PLD). In addition, these authors found conduction and valence band offsets to silicon of 2–2.5 eV. The thermal stability of $LaScO_3$, $GdScO_3$, and $DyScO_3$ thin films deposited with off-axial pulsed laser deposition was investigated by Zhao *et al.*[5] They showed that in contact with silicon the amorphous phase of $LaScO_3$ is stable up to 800 °C while $DyScO_3$ and $GdScO_3$ thin films remain amorphous up to 1000 °C. However, films deposited with PLD are inhomogeneous and exhibit many particulates on the surface that have chipped off from the target. Other techniques such as chemical vapor deposition normally use an oxidizing atmosphere at elevated temperatures to stoichiometrically deposit binary or ternary oxides. This leads to the growth of a thermal SiO_2 on silicon substrates preventing the realization of low equivalent oxide thicknesses. Because of little differences in the morphological and electrical properties of $DyScO_3$ and $GdScO_3$ and their superior thermal stability,[2–5] $GdScO_3$ has been exemplarily selected to investigate the deposition of thin films with an unconventional deposition technique for such a material.

In this work, gadolinium scandate thin films were deposited by means of electron beam evaporation in a conventional deposition chamber (Leybold Univex 450). Typically, with this technique complex stoichiometries cannot be transferred from the evaporation source to the substrate because of different vapor pressures of the elements involved. But since the vapor pressures of Gd and Sc are similar, a deposition of stoichiometric $GdScO_3$ thin films from a stoichiometric evaporation source made from a mixture of the metal oxides could be demonstrated. The depositions were performed at a pressure of $1-5\times10^{-6}$ mbar without addition of any process gas. These high vacuum conditions offer the possibility to deposit the scandate directly on silicon preventing the formation of a low-κ SiO_x interface layer.

As substrates, 2×2 cm^2 large pieces of (100) *p*-type silicon were used. Prior to the deposition either a 2 nm thick silicon dioxide was thermally grown on the surface or the substrate was HF dipped to remove the native oxide. The sample holder in the chamber is equipped with a resistive heater and the depositions were done at a substrate temperature of 600 °C. After deposition, the films were investigated with respect to their morphology and chemical composition by means of Rutherford backscattering spectrometry (RBS), x-ray reflectometry (XRR), high temperature x-ray diffraction (HT-XRD), transmission electron microscopy (TEM), and atomic force microscopy (AFM).

For electrical characterization of the films, capacitor stacks were manufactured. Metal top contacts (Au, Pd, or Pt) with a thickness of 70 nm and an area of 65×65 μm^2 were deposited by thermal or electron beam evaporation through a shadow mask. The Ohmic backside contact was realized by deposition of 200 nm Al followed by a forming gas anneal (10% H_2/90% N_2) to improve the backside contact and the high-κ dielectric-to-silicon interface. The capacitor stacks were investigated using an impedance analyzer (HP 4192A) for *C-V* measurements and a semiconductor parameter analyzer (HP 4155B) for leakage current measurements.

Figure 1 shows a cross sectional TEM micrograph of a 17 nm thick $GdScO_3$ film after deposition on a HF last sur-

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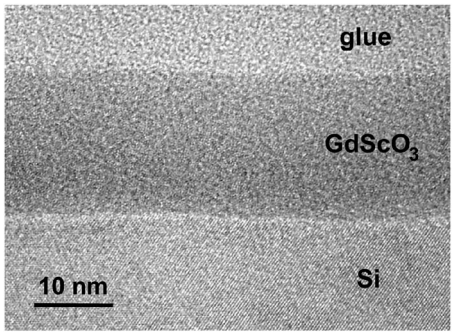

FIG. 1. TEM micrograph of a 17 nm thick $GdScO_3$ film deposited at 600 °C on a HF last surface of (100) Si.

face of (100) silicon at a substrate temperature of 600 °C. The film exhibits a homogeneous and amorphous structure. Obviously, the growth of an interfacial SiO_x layer was suppressed in the high vacuum conditions. The scandate layer directly adjoins the crystalline silicon substrate.

To investigate the stoichiometry of the films the coverage of the substrate with Gd and Sc atoms was determined using RBS. The stoichiometry of the films is close to the nominal composition of $GdScO_3$. The ratio Gd:Sc lies between 1:0.9 and 1:1.3. Within this range no influences of the stoichiometry on the morphology or electrical properties of the films could be observed. In addition, the RBS measurements confirm a growth rate linear with deposition time. Comparisons of RBS (coverage with atoms) and XRR data (physical thickness) show that the densitiy of the films deposited at 600 °C is about 83% of the single crystalline density.

The films are free from particulates and homogeneous. A film thickness variation of $<5\%$ over a 2 in. wafer was achieved. In addition, the surface is very smooth as indicated by AFM measurements (Fig. 2). A peak-to-valley roughness of about 1 nm and a rms roughness of below 0.1 nm for film thicknesses up to 20 nm within a scan size of 2×2 μm^2 were revealed.

To investigate the thermal stability of the scandate films, *in situ* high temperature XRD measurements were performed in high vacuum ambient. The sample is held at each temperature step for 30 min to perform the measurement. Figure 3 shows data of a 20 nm thick $GdScO_3$ film deposited at 600 °C on a HF last surface. Obviously the layer remains amorphous up to 1000 °C. At 1100 °C, a phase segregation

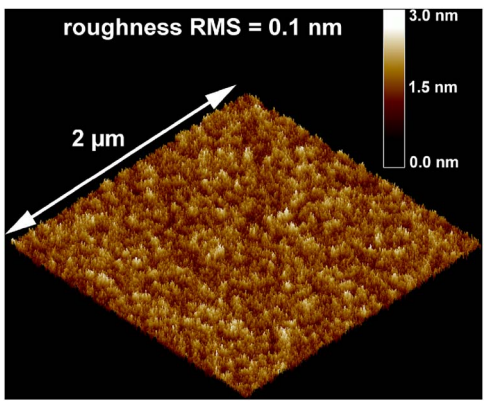

FIG. 2. (Color online) AFM scan of an ≈20 nm thick $GdScO_3$ film; the scan size is 2×2 μm^2, the peak-to-valley value 1 nm, and the RMS roughness 0.1 nm.

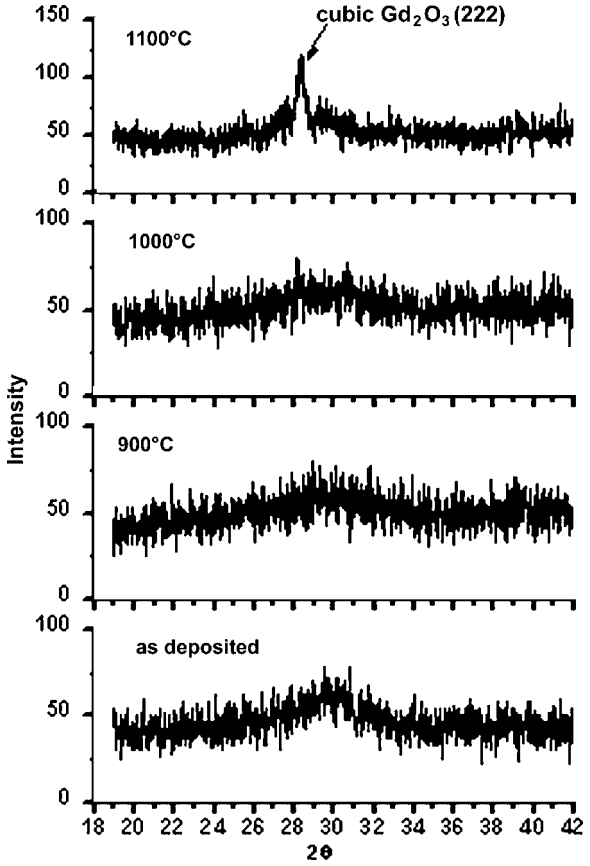

FIG. 3. High temperature XRD measurement of an ≈20 nm thick $GdScO_3$ film deposited on a HF last surface of (100) Si at 600 °C.

occurs and Gd_2O_3 crystallites start to form. This crystallization onset temperature is much higher than that for hafnium dioxide[6] films. In addition, a decomposition of the films as reported for hafnium dioxide films in literature[7] could not be observed. Compared to the films prepared by PLD,[5] the e-beam films show a similar crystallization onset temperature. The crystalline phase, however, is cubic Gd_2O_3, instead of hexagonal Gd_2O_3, as found in the PLD films.[4] The high crystallization onset temperature is within the thermal budget required for CMOS processing.

For the electrical characterization, samples with different film thicknesses (3.8, 6, 10, and 19.5 nm) were prepared and Pt top contacts were deposited to form capacitor stacks. On all samples, *C-V* and *I-V* measurements were performed. Figure 4 displays *I-V* data for this set of samples. The curves were recorded with a hold time of 30 s for each measuring point to wait for all relaxation processes to be decayed before the measurement. The capacitance equivalent thickness (CET) of the capacitors calculated from the capacitance in accumulation at −2 V ranges from 1.5 to 2.4 nm. In contrast to the equivalent oxide thickness (EOT) the CET does not take quantum effects into account and usually is significantly larger for thin films. The thinnest film with a CET of 1.5 nm exhibits a low leakage current density of 7.7×10^{-4} A/cm^2 at a voltage of −2 V which is about five orders of magnitude lower than conventional SiO_2.

The leakage current of the thicker films is close to the detection limit. The inset in Fig. 4 shows a typical *C-V* curve of the film with a CET of 2.4 nm. It was recorded at 100 kHz with a hold time of 3 s for each measuring point. It is free of humps and irregularities and exhibits a small hysteresis indi-

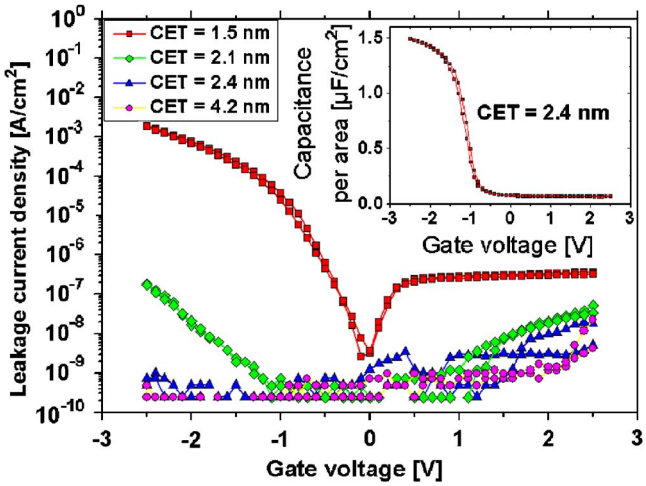

FIG. 4. (Color online) *I-V* curves of $GdScO_3$ films with different thicknesses; the inset shows a *C-V* curve for the sample with a CET of 2.4 nm recorded at 100 kHz.

cating a low number of interface states. With the two-frequency method an interface trap charge density of the films close to 5×10^{11} cm^{-2} was determined.

In Fig. 5 the capacitance equivalent thickness of the gate stacks is plotted versus the film thickness determined by XRR measurements. The data shown are from two different sample series on HF last surface with different top contact metals (Pd and Pt). All the data points lie on a straight line.

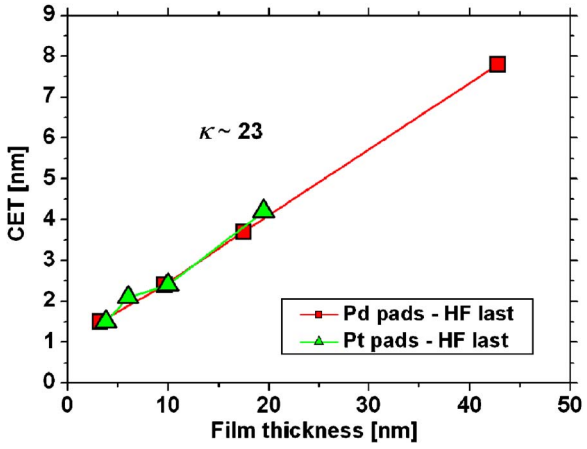

FIG. 5. (Color online) CET plots of sample series on HF last surface with different top contact metals. From the slope of the plots a κ value of $\approx$23 can be derived.

No significant difference between the different contact pads is observed. From the slope of the linear fit a κ value of $\approx$23 is derived which is comparable to HfO_2.[7] CET plots of samples on thermal oxide or HF last surface with Au top contacts reveal similar κ values (not shown). The intersect of the plots with the CET axis at 0.9 nm indicates the existence of a thin interfacial layer between the high-κ dielectric and the silicon substrate with a dielectric constant lower than $GdScO_3$. The possible origin of such a layer has still to be analyzed. A detailed investigation on the interface morphology and the possibilities for modification by variation of the deposition and annealing parameters is in progress.

In summary, with electron beam evaporation a stoichiometric transfer of gadolinium scandate thin films from a stoichiometric ceramic source in ultrahigh vacuum conditions could be demonstrated. The films show very promising properties for high-κ applications. Homogeneous and particulate free depositions linear with time were achieved. The surface of the films is very smooth (rms roughness $<$0.1 nm). *In situ* high temperature XRD measurements proved an excellent thermal stability of the amorphous phase up to 1000 °C. TEM micrographs show a SiO_x free interface on HF dipped silicon after deposition. The electrical investigations reveal low leakage current densities (770 $\mu A/cm^2$ for a CET of 1.5 nm) *C-V* curves with a small hysteresis and a dielectric constant of $\approx$23 independent of the gate metal used.

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